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EXAMINER	
CASCHERA, ANTONIO A	
ART UNIT	**PAPER NUMBER**
2676	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/747,966	**Applicant(s)** PALLISTER, KIM	
	Examiner Antonio A. Caschera	**Art Unit** 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-22* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 2, 4, 18, 19 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Dye et al. (U.S. Patent 6,366,290 B1).

In reference to claims 1 and 18, Dye et al. discloses a graphics engine for improving texture mapping implementing a selectable mode filter (see column 3, lines 24-25). Dye et al. discloses the texturing process to include receiving x, y pixel coordinates and converting the coordinates to fractional u, v texel coordinates, to access texel values from a texture memory (see column 6, lines 41-51). Dye et al. further discloses the selectable mode filter to combine texel values from texture memory to compute a single texel output value which is then used to render the pixel associated with the x, y pixel address (see column 6, lines 51-64). Note, the office interprets the selectable mode filter of Dye et al., functionally equivalent to the programmable filter of applicant's claims. Further note, the filtered texel value for the specific pixel is outputted in reference to "TEXEL_OUT" of Figure 4 of Dye et al. Also, in reference to claim 18, Dye et al. discloses a computer readable storage medium for storing an executable set of software instructions performing the above texturing techniques, when executed (see column 38,

lines 65-67). Note, in view of the Applicant being his own Lexicographer (defining the term "programmable filter," see *Response to Arguments* below), the office adds to the previous interpretation of the filtering of Dye. In particular, the office points to Figure 8 and columns 7-8, lines 66-9 in Dye wherein different algorithms, i.e. two texel or four texel averaging, are executed. Even further, Figure 8 shows a state machine of the programming of the filter directing the operation of the system of Dye to perform point sampling, two texel or four texel averaging by providing three separate control paths for these three different operations (see column 13, lines 28-35). Clearly, Dye discloses the system and filter, "capable of executing a software program" since either a point sampling, two texel or four texel averaging algorithm is executed. Also, the office interprets these averaging techniques to inherently comprise of, "...one or more instructions from a defined instruction set," as computing the average of values necessitates at least an addition operation, which is a common instruction as indicated in Table 1 of Applicant's specification. Therefore, the office interprets Dye to teach the programmable filter limitation, as defined by the Applicant.

In reference to claims 2 and 19, Dye et al. discloses all of the claim limitations as applied to claims 1 and 18 respectively above in addition, Dye et al. discloses filtering the texel values to comprise of reading control signals produced from a selectable filter address selection unit (see #200 and 400 of Figure 4, #400 receives control signals, SCALE FACTOR, LOAD, ACCUMULATE, TEX_1) which the office interprets functionally equivalent to a control register since it maintains control signals (see column 7, lines 53-61). Dye et al. also discloses the selectable filter address selection unit to maintain fractional portions of the u, v texture address and produces output texture address values (see column 7, lines 10-14, 28-30 and #200,

"u_out" and "v_out" of Figure 4). The "u_out" and "v_out" signals are interpreted by the office as equivalent to "source" data and therefore are specified within the selectable filter address unit.

In reference to claims 4 and 21, Dye et al. discloses all of the claim limitations as applied to claims 1 and 18 respectively above in addition, Dye et al. discloses sending u_frac and v_frac, fractional data to multiple logic units, "mask logic" and "math logic" (see #210, 240, "U_FRAC" and "V_FRAC" of Figure 5). Note, the office interprets that these logic units of Dye et al. are functionally equivalent to a "plurality of registers" according to the definition of register, defined by Merriam-Webster's Collegiate Dictionary, 10th ed. (© 2002, Merriam-Webster, Inc. see "[1]register" page 982), "register 9: a device (as in a computer) for storing small amounts of data; one in which data can be both stored and operated on." Since, the fractional data in the logic units of Dye et al. is at least temporarily stored and operated on, the office interprets the logic units of Dye et al. to function equivalent to a computer register therefore, the plurality of logic units is seen equivalent to the "plurality of registers" of applicant's claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye et al. (U.S. Patent 6,366,290 B1).

In reference to claims 3 and 20, Dye et al. discloses all of the claim limitations as applied to claims 1 and 18 respectively above. Dye et al. discloses receiving x and y pixel data representing vertices of a polygon (see column 1, lines 46-50 and column 6, lines 45-47). Note, the office interprets that Dye et al. inherently discloses some sort of vertex unit for derivation of coordinate data since Dye et al. discloses implementing the texturing techniques using a computer (see column 1, lines 19-20) which commonly comprise of some sort of functionally equivalent vertex deriving element. Dye et al. does not explicitly disclose receiving x, y and z coordinate data. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement the above techniques of Dye et al. within a 3D rendering display environment thereby defining pixel data in three dimensions, x, y and z. Applicant has not disclosed that the specific application of three dimensions in defining pixel data provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the texturing techniques of Dye et al. using 2D pixel data because the use of either two or three dimensions to define pixel data is a matter of design choice as preferred by the designer and to which best suits the application at hand. For example, for solid modeling texturing techniques a designer of a system might be inclined to include calculations in three dimensions while the designer might only choose to implement two dimensional calculations for "photographic" modes of texture, in order to reduce calculations and system costs. Therefore, it would have been obvious to one of ordinary skill in this art to modify Dye et al. to obtain the invention as specified in claims 3 and 20.

3. Claims 5, 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye et al. (U.S. Patent 6,366,290 B1) in view of Tang et al. (U.S. Patent 6,867,778 B2).

In reference to claims 5 and 22, Dye et al. discloses all of the claim limitations as applied to claims 1 and 18 respectively above. Dye et al. does not explicitly disclose writing the filtered texel value to a register however Tang et al. does. Tang et al. discloses a system and method for rendering a triangle such as a polygon (see column 3, lines 2-3) wherein a filtered texture value is stored within a texture buffer (see column 9, lines 1-11, 26-29, 36-38 and #170, 178, 186 and 20 of Figure 5 of Tang et al.). Tang et al. also discloses filtered data being transferred by a pixel transfer unit to the texture buffer, via a texture buffer MUX (see column 9, lines 26-29), therefore the office interprets that Tang et al. inherently discloses notifying the texture MUX when a filtered value is available because the pixel transfer unit decides on whether to transfer the data to the texture buffer through the texture MUX, which therefore inherently knows whether new data is received. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the texture storing techniques of Tang et al. with the texture filtering techniques of Dye et al. in order to create a processor like graphics subsystem, allowing for processing power, that would normally be used by a CPU, to be handled by the graphics subsystem, increasing overall system performance (see column 1, lines 29-34 of Tang et al.).

In reference to claim 6, Dye et al. discloses a graphics engine for improving texture mapping implementing a selectable mode filter (see column 3, lines 24-25). Dye et al. discloses the texturing process to include receiving x, y pixel coordinates and converting the coordinates to fractional u, v texel coordinates, to access texel values from a texture memory (see column 6,

lines 41-51). Dye et al. further discloses the selectable mode filter to combine texel values from texture memory to compute a single texel output value which is then used to render the pixel associated with the x, y pixel address (see column 6, lines 51-64). Note, the office interprets the selectable mode filter of Dye et al., functionally equivalent to the programmable filtering module of applicant's claim. Dye et al. does not explicitly disclose a fragment processing module communicating with the filtering module however Tang et al. does. Tang et al. discloses a system and method for rendering a triangle such as a polygon (see column 3, lines 2-3) wherein a filtered texture value is stored within a texture buffer (see column 9, lines 1-11, 26-29, 36-38 and #170, 178, 186 and 20 of Figure 5 of Tang et al.). Tang et al. also discloses a fragment processor connected to a filtering unit, via other various modules, for performing standard fragment processing operations (see column 9, lines 39-40 and #180, 184 of Figure 5). Tang et al. discloses a frame buffer storing display data and a pixel transfer unit and texture environment MUX for blending texture data with already existing texture buffer data (see column 9, lines 7-15 and 26-29 and Figure 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the texture storing techniques of Tang et al. with the texture filtering techniques of Dye et al. in order to create a processor like graphics subsystem, allowing for processing power, that would normally be used by a CPU, to be handled by the graphics subsystem, increasing overall system performance (see column 1, lines 29-34 of Tang et al.).

4. Claims 7, 8, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye et al. (U.S. Patent 6,366,290 B1), Tang et al. (U.S. Patent 6,867,778 B2) and further in view of Emberling (U.S. Pub 2004/0227765 A1).

In reference to claim 7, Dye et al. and Tang et al. disclose all of the claim limitations as applied to claim 6 above. Neither Dye et al. nor Tang et al., explicitly disclose the texture filtering module comprising of a plurality of control, source and temporary registers and at least one output register however Emberling does. Emberling discloses a method of improving texture cache access in a graphics system (see paragraph 2 and title). Emberling discloses the graphics system comprising of a programmable filtering engine supporting multiple modes (see paragraph 113, lines 1-7) wherein the filtering engine includes a system of digital circuits, including registers for storing numerous variables (see paragraphs 118-119). Specifically, Emberling discloses registers for programming values of the pseudo code found in paragraph 118 (see paragraphs 118 and lines 10-13 of paragraph 119). The office interprets the Xp, Yp values equivalent to source values as they represent the current pixel position (see paragraph 119, lines 1-5) and therefore, are inherently stored in a plurality of source registers (Xp, Yp source registers). Also, the office interprets the M, Xstart and Ystart values equivalent to control values as they define the characteristics of the filter (see paragraph 118, lines 3-12) and therefore, are inherently stored in control registers (M, Xstart, Ystart control registers). Even further, counter variables, I, J (see pseudo code of paragraph 118) are interpreted as temporary variables and are therefore inherently stored in temporary registers. Finally, Emberling discloses outputting the filtered pixel values to a buffer, which the office interprets equivalent to the output register (see paragraph 119, lines 5-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the filtering architecture of Emberling with the texture storing techniques of Tang et al. and texture filtering techniques of Dye et al. in order to create a texture memory accessing system that performs very quickly, improving speed and

efficiency of memory accesses of texture data from texture memory (see paragraph 8, lines 1-5 of Emberling) (further see *Response to Arguments* below).

In reference to claim 8, Dye et al., Tang et al., Dye et al. and Emberling disclose all of the claim limitations as applied to claim 7 above in addition, Emberling discloses that texture mapping is generally a read-only operation (see paragraph 9, lines 7-8) therefore, the office interprets Emberling to inherently disclose source storage to be read-only.

In reference to claim 11, Dye et al. and Tang et al. disclose all of the claim limitations as applied to claim6 above however, neither Dye et al. nor Tang et al. explicitly disclose the filtering unit as a plurality of processing cores executing an instruction set. Emberling discloses a method of improving texture cache access in a graphics system (see paragraph 2 and title). Emberling discloses the graphics system comprising of a programmable filtering engine supporting multiple modes (see paragraph 113, lines 1-7) wherein the filtering engine comprises of multiple filtering units (see Figure 11 FU(0)-FU(3)), configured to execute filtering on video streams based upon instructions from host software (see paragraph 119, lines 12-15 and paragraphs 121-122). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the filtering architecture of Emberling with the texture storing techniques of Tang et al. and texture filtering techniques of Dye et al. in order to create a texturing memory accessing system that performs very quickly, improving speed and efficiency of memory accesses of texture data from texture memory (see paragraph 8, lines 1-5 of Emberling).

In reference to claim 12, Dye et al. and Tang et al. disclose all of the claim limitations as applied to claim 11 above however, neither Dye et al. nor Tang et al. explicitly disclose the

plurality of cores executing a filtering program on at least one pixel in parallel however Emberling does. Emberling discloses a method of improving texture cache access in a graphics system (see paragraph 2 and title). Emberling discloses the graphics system comprising of a programmable filtering engine supporting multiple modes (see paragraph 113, lines 1-7) wherein the filtering engine comprises of multiple filtering units (see Figure 11 FU(0)-FU(3)), configured to execute filtering on video streams based upon instructions from host software (see paragraph 119, lines 12-15 and paragraphs 121-122). Emberling further discloses the filtering units to perform filtering upon two video streams in parallel (streams A and B) (see paragraph 121, last 3 lines and Figure 11) which the office interprets as inherently comprising at least two pixels. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the filtering architecture of Emberling with the texture storing techniques of Tang et al. and texture filtering techniques of Dye et al. in order to create a texturing memory accessing system that performs very quickly, improving speed and efficiency of memory accesses of texture data from texture memory (see paragraph 8, lines 1-5 of Emberling).

5. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis et al. (U.S. Patent 6,731,296 B2) in view of Tang et al. (U.S. Patent 6,867,778 B2).

In reference to claim 13, Lewis et al. discloses a method and system for processing textures for a graphical image on a display which includes fragments of objects (see column 2, lines 55-58). Lewis et al. discloses a memory and a plurality of texture processors coupled with the memory (see column 2, lines 58-60). Lewis et al. also discloses the texture processors to process/blend/filter according to a certain program (see column 8, lines 19-26). Note, the office interprets that the texture processors of Lewis et al. perform functionally equivalent to the

"programmable filter" of Applicant's claim since the processors in Lewis et al. operate according to a program, which had to be coded, and are therefore programmable. Lewis et al. discloses displaying the textured fragments on a display device in raster order (see column 7, lines 50-57). Lewis et al. does not explicitly disclose a fragment processing module to apply filtered data to a fragment however Tang et al. does. Tang et al. discloses a system and method for rendering a triangle such as a polygon (see column 3, lines 2-3) wherein a filtered texture value is stored within a texture buffer (see column 9, lines 1-11, 26-29, 36-38 and #170, 178, 186 and 20 of Figure 5 of Tang et al.). Tang et al. also discloses a fragment processor performing standard fragment processing operations along with a texture environment unit performing additional filtering techniques upon buffered texture data (see column 9, lines 11-15, 39-40 and #180, 184 of Figure 5)), the combination of these units interpreted by the office as functionally equivalent to the fragment processing module of applicant's claims. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the texturing techniques of Tang et al. with the texture filtering architecture of Lewis in order to create a processor like graphics subsystem, allowing for processing power, that would normally be used by a CPU, to be handled by the graphics subsystem, increasing overall system performance (see column 1, lines 29-34 of Tang et al.).

In reference to claim 14, Lewis et al. and Tang et al. disclose all of the claim limitations as applied to claim 13 above. Since both Lewis et al. and Tang et al. disclose implementing their inventions using a computer system (see column 6, lines 41-43 of Lewis et al. and column 4, lines 52-59 of Tang et al.) the office interprets that both Lewis et al. and Tang et al. inherently

disclose the fragment processor and texture processor integrated with a host processor as computer systems usually employ host CPU's.

In reference to claim 15, Lewis et al. and Tang et al. disclose all of the claim limitations as applied to claim 13 above in addition, Lewis et al. discloses the texture processors comprised within a texture unit (see #150 of Figure 6 and #154-n of Figure 7) which is further comprised within an image generating unit (see #120 of Figure 6) while Tang et al. discloses the fragment processor and texture environment unit comprised within a hardware accelerator (see columns 8-9, lines 65-15 and Figure 5). Note, the office interprets the image generating unit and hardware accelerator functionally equivalent to the graphics coprocessor of Applicant's claim.

In reference to claim 16, Lewis et al. and Tang et al. disclose all of the claim limitations as applied to claim 13 above. Lewis et al. also discloses the texture processors able to access a set of registers instead of the crossbar shown in Figure 7 (see column 8, lines 38-40).

In reference to claim 17, Lewis et al. and Tang et al. disclose all of the claim limitations as applied to claim 15 above in addition, Tang et al. discloses implementing an AGP port coupling the graphics subsystem to system memory (see column 5, lines 54-58).

Allowable Subject Matter

6. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In reference to claim 9, the prior art of record (Dye et al. (U.S. Patent 6,366,290 B1), Tang et al. (U.S. Patent 6,867,778 B2), Lewis et al. (U.S. Patent 6,731,296 B2) and Emberling

(U.S. Pub 2004/0227765 A1)) does not explicitly disclose the plurality of control registers comprising a status register, an address register, an offset register and a plurality of fraction registers, in combination with the further limitations of claim 7, of which claim 9 is dependent upon.

In reference to claim 10, the prior art of record (Dye et al. (U.S. Patent 6,366,290 B1), Tang et al. (U.S. Patent 6,867,778 B2), Lewis et al. (U.S. Patent 6,731,296 B2) and Emberling (U.S. Pub 2004/0227765 A1)) does not explicitly disclose the plurality of control registers comprising at least one sampling register having a bit corresponding to each of the source registers to indicate if sampling of a corresponding source register is required, in combination with the further limitations of claim 7, of which claim 10 is dependent upon.

Response to Arguments

7. Applicant's arguments, see page 7 of Applicant's Remarks, filed 06/13/05, with respect to the objection of the drawings have been fully considered and are persuasive. The objection of the drawings has been withdrawn since informalities concerning the reference numbers have been corrected for.

8. Applicant's arguments, see page 7 of Applicant's Remarks, filed 06/13/05, with respect to the 112 2nd paragraph rejection of claim 12 have been fully considered and are persuasive. The 112 2nd paragraph rejection of the claim 12 has been withdrawn since antecedent basis has been corrected for.

9. Applicant's arguments, see pages 9-10, filed 06/13/05, with respect to the rejection(s)of claim(s) 13-17 under 35 USC 103(a) have been fully considered and are persuasive. Therefore,

the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Lewis et al..

10. Applicant's arguments filed 06/13/05 have been fully considered but they are not persuasive.

In reference to claims 1-4 and 18-21, Applicant argues that neither the Dye nor Tang references explicitly teach "filtering the texel values through a programmable filter," (see pages 7-8 of Applicant's Remarks). Applicant goes on to explain that the term "programmable filter" has been defined in the specification (see paragraph 13) as, "capable of executing a software program consisting of one or more instructions from a defined instruction set," (see page 8, 1st paragraph of Applicant's Remarks). In view of the Applicant being his own Lexicographer, the office adds to the previous interpretation of the filtering of Dye. In particular, the office points to Figure 8 and columns 7-8, lines 66-9 in Dye wherein different algorithms, i.e. two texel or four texel averaging, are executed. Even further, Figure 8 shows a state machine of the programming of the filter directing the operation of the system of Dye to perform point sampling, two texel or four texel averaging by providing three separate control paths for these three different operations (see column 13, lines 28-35). Clearly, Dye discloses the system and filter, "capable of executing a software program" since either a point sampling, two texel or four texel averaging algorithm is executed. Also, the office interprets these averaging techniques to inherently comprise of, "...one or more instructions from a defined instruction set," as computing the average of values necessitates at least an addition operation, which is a common instruction as indicated in Table 1 of Applicant's specification. Therefore, the office interprets Dye to teach the programmable filter limitation, as defined by the Applicant.

In reference to claims 5 and 22, Applicant argues that neither the Dye nor Tang references explicitly teach "filtering the texel values through a programmable filter," (see pages 7-8 of Applicant's Remarks). The office points out that the Tang reference is incorporated to explicitly show the writing of filtered texture values to a register. In view of the above arguments as applied to Dye, the office interprets such arguments in view of Tang moot due to the new grounds of rejection in view of Dye.

In reference to claims 7, 8, 11 and 12, Applicant argues that the Emberling filter is not a programmable filter and does not filter texture data (see page 10 of Applicant's Remarks). Although, the filter of Emberling may not filter texture data and may not be "programmable" as defined by the Applicant, the office points out that the Emberling reference was incorporated to show the limitation of a filtering module comprising of a plurality of control, source and temporary registers and at least one output register. The office believes that the filter and associated registers in Emberling are applicable to any type of operable data, i.e. texture data, especially since Emberling filters pixel data making up a video stream. Therefore, the office maintains its current rejection based upon Emberling.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (571) 272-7781. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella, can be reached at (571) 272-7778.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

aac

8/16/05

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
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